

**Notice of References Cited**

Application/Control No.

09/683,677

Applicant(s)/Patent Under  
Reexamination  
DEVINS ET AL.

Examiner

Saif A. Alhija

Art Unit

2128

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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*	B	US-5,600,579	02-1997	Steinmetz, Jr., William C.	703/13
*	C	US-5,805,605	09-1998	Lee et al.	714/718
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**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
*	U	"An Embedded PowerPC SOC for Test and Measurement Applications", 2000 IEEE, Blaner et al.
*	V	Dutta et al. "Viper". September-October 2001. IEEE.
*	W	"System and Method Relating to Verification of Integrated Circuit Design" W00201424 , 06/2001
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.